NASA TECH BRIEF

Highly Linear, Sensitive Analog-to-Digital Converter

$$+10V = 111 \text{-------} 1$$
$$0V = 100 \text{-------} 0$$
$$-10V = 111 \text{---} 0$$
$$LSB = \frac{20V}{2n} = \frac{20V}{2^{13}} = 2.4414 \text{ mV}$$
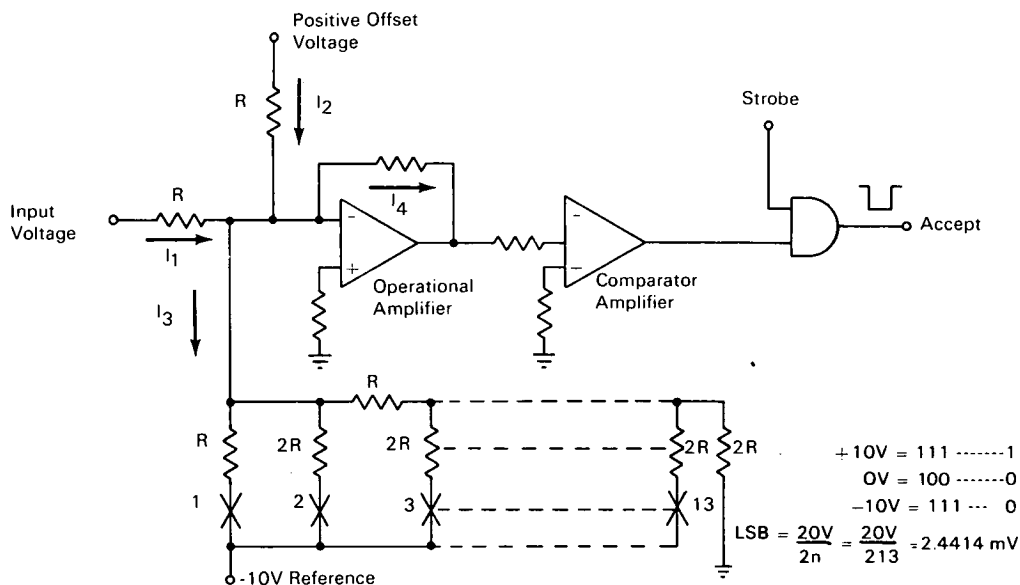
The analog-to-digital (A/D) converter shown in the schematic was designed to convert a ± 10 volt full scale input signal into a 13 bit digital output. The converter has a least significant bit (LSB) weight of 2.4414 mV and is extremely linear (nonlinearity of 0.0075 percent of full scale) over the temperature range of 0° to 70°C. Other advantages of the converter, in addition to its high sensitivity and linearity, are its low quantizing error (± 1/2 of the LSB, or ± 1.2207 mV), its high resistance to mechanical shock and vibration loads, and its temporary data storage capabilities. It has a moderate conversion speed of 20 microseconds per bit, but has been operated equally well at a 10 microsecond bit rate.

The A/D converter incorporates a very stable, regulated –10 volt ladder reference supply and a positive offset voltage supply. The offset voltage effectively shifts the ± 10 volt input signal to a 0 volt to +20 volt input signal at the summing junction of the operational amplifier. The most significant bit (MSB) of the ladder is the sign bit; its current contribution to the summing junction is equal in magnitude but opposite in sign to that of the offset voltages. Output of the A/D converter is in offset binary code corresponding to various voltage inputs, as exemplified below:

Voltage Input	Code
+ 10	1111----11
+ LSB	1000----01
0	1000----00
- LSB	0111----11
- 10	0000----00

When a voltage appears at the input terminal, the MSB of the ladder is switched from gound to the –10 volt reference supply. If the sum of the input currdnt (I_1) and the offset current (I_2) is greater than the current (I_3) furnished by the MSB, the output of the operational amplifier goes negative, so that the feedback current (I_4) will balance the currents at the summing junction. The output of the comparator, which is operated open loop, thus goes positive. At the end of the 20 microsecond comparison time, a strobe pulse is generated and an "accept" pulse sets a flip-flop to hold on the MSB switch. The second bit is then tried. If the sum of the input and offset currents is less than the sum of the two MSB currents, the second bit will be rejected. The cycle continues until all 13 bits have been tried and accepted or rejected. The digital data are stored in the memory flip-flops which control the ladder switches. These data are available for use until the flip-flops are cleared prior to another conversion.

Notes:

1. The A/D converter was designed for use in a system that takes four samples of a measurement parameter. These samples are combined into a ratio formula to cancel the converter gain and offset errors; the ratio formula therefore depends only on the linearity of the converter.

2. The first two legs of the 13 bit ladder are external to the conventional 11 bit ladder network. This arrangement improves system accuracy by trimming out the error due to voltage drop across the switches.

3. The converter employs a gain switch in the feedback loop of the operational amplifier. For output voltages from this amplifier greater than 0.5 V, the gain is unity, which prevents the operational amplifier from saturating (thus eliminating the time that would be required for it to become unsaturated). For output voltages less than 0.5 V, the gain is 20 to increase the sensitivity of the comparator amplifier.

4. The converter can be temperature-compensated to stabilize gain and offset errors. It could then be used for absolute voltage measurements to an accuracy of 0.01 percent.

5. This information is complete in itself. No additional documentation is available.

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20564.